

## 74F74 Dual D-Type Positive Edge-Triggered Flip-Flop

### General Description

The F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

### Asynchronous Inputs:

- LOW input to  $\bar{S}_D$  sets Q to HIGH level
- LOW input to  $\bar{C}_D$  sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

### Features

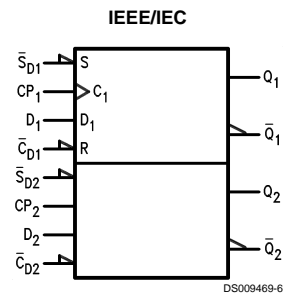
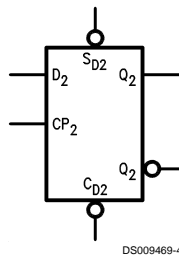
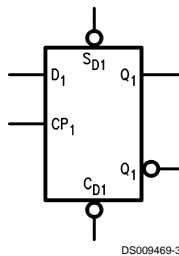
- Guaranteed 4000V minimum ESD protection

### Ordering Code:

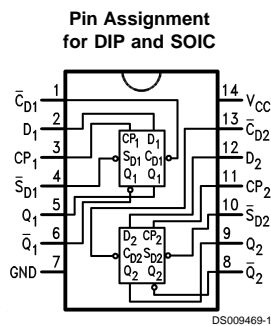
Commercial	Package Number	Package Description
74F74PC	N14A	14-Lead (0.300" Wide) Molded Dual-In-Line
74F74SC (Note 1)	M14A	14-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F74SJ (Note 1)	M14D	14-Lead (0.300" Wide) Molded Small Outline, EIAJ

Note 1: Devices also available in 13" reel. Use Suffix = SCX.

### Logic Symbols



### Connection Diagram



## Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$D_1, D_2$	Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$CP_1, CP_2$	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{C}_{D1}, \overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	1.0/3.0	20 $\mu$ A/-1.8 mA
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs (Active LOW)	1.0/3.0	20 $\mu$ A/-1.8 mA
$Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$	Outputs	50/33.3	-1 mA/20 mA

## Truth Table

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	$\nearrow$	h	H	L
H	H	$\searrow$	l	L	H
H	H	L	X	$Q_0$	$\overline{Q}_0$

H (h) = HIGH Voltage Level

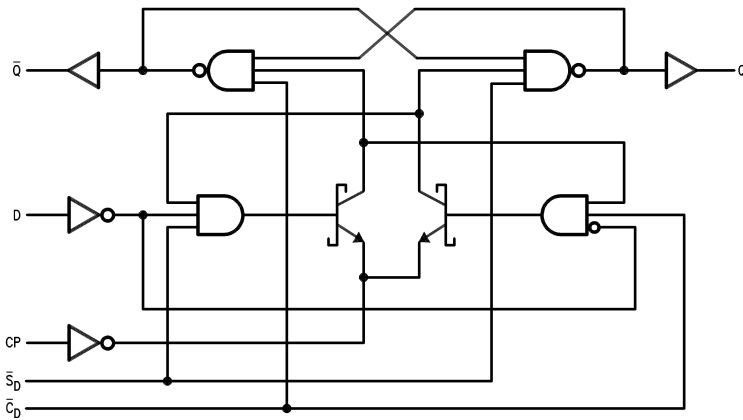
L (l) = LOW Voltage Level

X = Immaterial

$Q_0$  = Previous Q ( $\overline{Q}$ ) before LOW-to-HIGH Clock Transition

Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

## Logic Diagram



DS009469-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential	
Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	

in LOW State (Max)                      twice the rated I<sub>OL</sub> (mA)  
ESD Last Passing Voltage (Min)                      4000V

## Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	74F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	74F		5.0	µA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	74F		7.0	µA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	74F		50	µA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 µA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	µA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -1.8	mA	Max	V <sub>IN</sub> = 0.5V (D, CP) V <sub>IN</sub> = 0.5V ( $\overline{C}_D$ , $\overline{S}_D$ )
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		10.5	16.0	mA	Max	

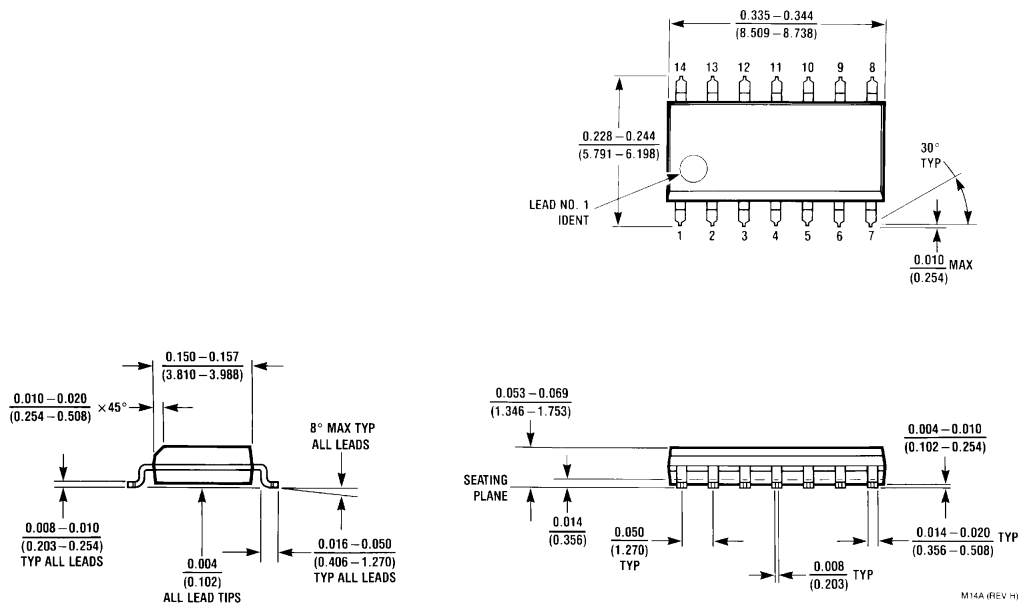
## AC Electrical Characteristics

Symbol	Parameter	74F			74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	100	125		100		MHz	
t <sub>PLH</sub>	Propagation Delay	3.8	5.3	6.8	3.8	7.8	ns	
t <sub>PHL</sub>	CP <sub>n</sub> to Q <sub>n</sub> or $\overline{Q}_n$	4.4	6.2	8.0	4.4	9.2	ns	
t <sub>PLH</sub>	Propagation Delay	3.2	4.6	6.1	3.2	7.1	ns	
t <sub>PHL</sub>	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q <sub>n</sub> or $\overline{Q}_n$	3.5	7.0	9.0	3.5	10.5	ns	

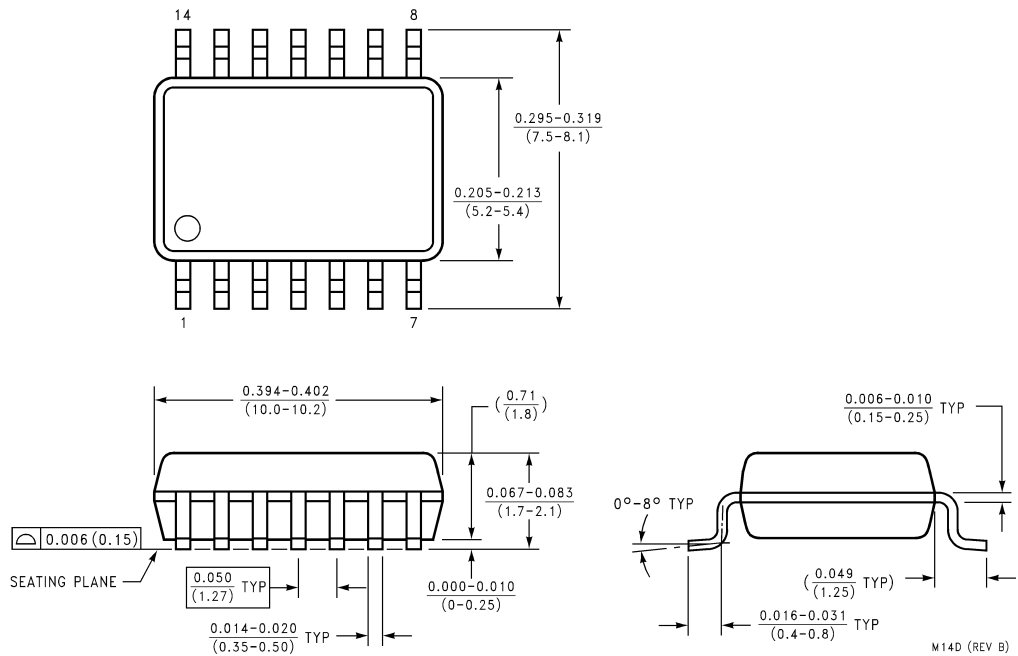
## AC Operating Requirements

Symbol	Parameter	74F		74F		Units	Fig. No.
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Com			
		Min	Max	Min	Max		
t <sub>s</sub> (H)	Setup Time, HIGH or LOW	2.0		2.0		ns	
t <sub>s</sub> (L)	D <sub>n</sub> to CP <sub>n</sub>	3.0		3.0			
t <sub>h</sub> (H)	Hold Time, HIGH or LOW	1.0		1.0			
t <sub>h</sub> (L)	D <sub>n</sub> to CP <sub>n</sub>	1.0		1.0		ns	
t <sub>w</sub> (H)	CP <sub>n</sub> Pulse Width	4.0		4.0			
t <sub>w</sub> (L)	HIGH or LOW	5.0		5.0		ns	
t <sub>w</sub> (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.0		4.0			
t <sub>rec</sub>	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0		2.0		ns	

**Physical Dimensions** inches (millimeters) unless otherwise noted

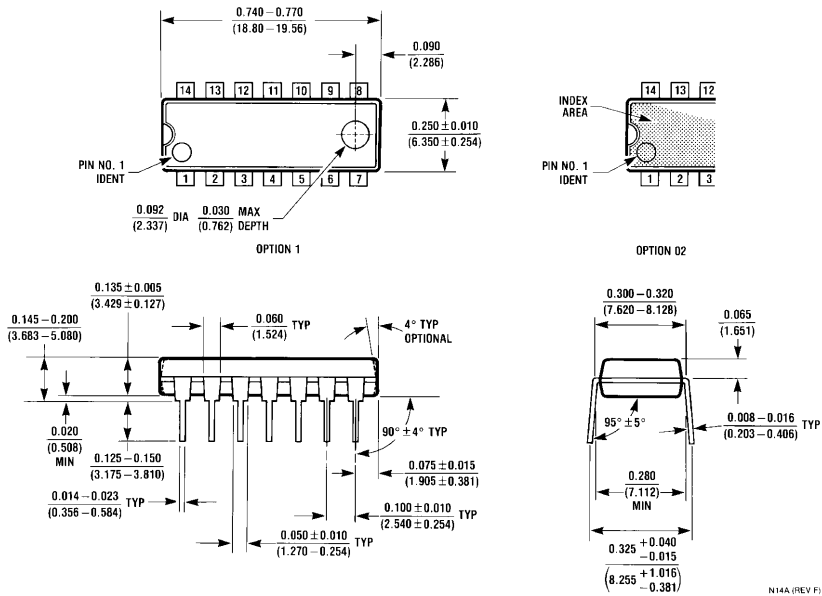


**14-Lead (0.150" Wide) Molded Small Outline, JEDEC (S)  
Package Number M14A**



**14-Lead (0.300" Wide) Molded Small Outline, EIAJ (SJ)  
Package Number M14D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Lead (0.300" Wide) Molded Dual-In-Line Package (P)**  
Package Number N14A

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