

# Latch/flip-flop

# 74F533, 74F534

74F533 Octal Transparent Latch, Inverting (3-State)  
 74F534 Octal D Flip-Flop, Inverting (3-State)

## FEATURES

- 8-bit transparent latch – 74F533
- 8-bit positive edge-triggered register – 74F534
- 3-State inverting output buffers
- Common 3-State Output register
- Independent register and 3-State buffer operation

## DESCRIPTION

The 74F533 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ( $\overline{OE}$ ) control gates.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ( $\overline{OE}$ ) controls all eight 3-State buffers independent of the latch operation. When  $\overline{OE}$  is Low, the latched or transparent data appears at the outputs. When  $\overline{OE}$  is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F534 is an 8-bit edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ( $\overline{OE}$ ) control gates.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's  $\overline{Q}$  output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ( $\overline{OE}$ ) controls all eight 3-State buffers independent of the latch operation. When  $\overline{OE}$  is Low, the latched or transparent data appears at the outputs. When  $\overline{OE}$  is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F533	5.5ns	41mA

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F534	165MHz	51mA

## ORDERING INFORMATION

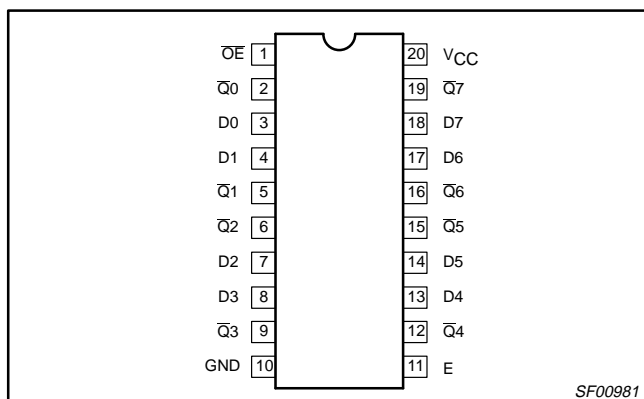
DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^\circ C$ to $+70^\circ C$
20-Pin Plastic DIP	N74F533N, N74F534N
20-Pin Plastic SOL	N74F533D, N74F534D

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

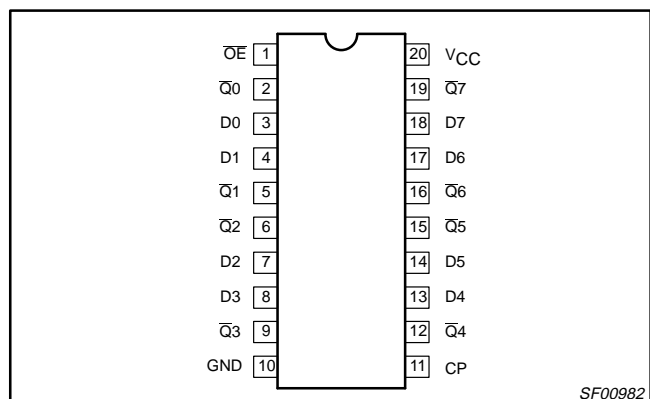
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
E (74F533)	Enable input (active High)	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20 $\mu$ A/0.6mA
CP (74F534)	Clock Pulse input (active rising edge)	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{Q}0 - \overline{Q}7$	Data outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

## PIN CONFIGURATION – 74F533



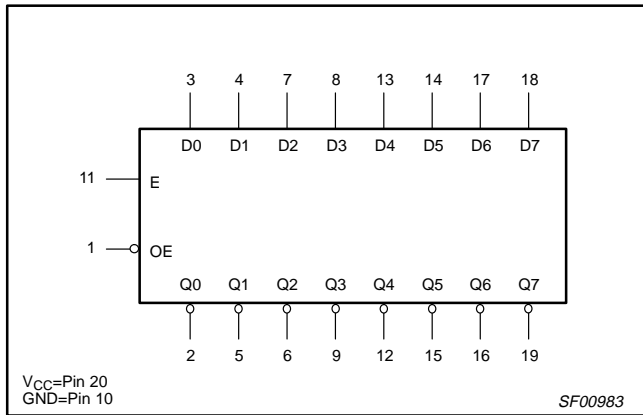
## PIN CONFIGURATION – 74F534



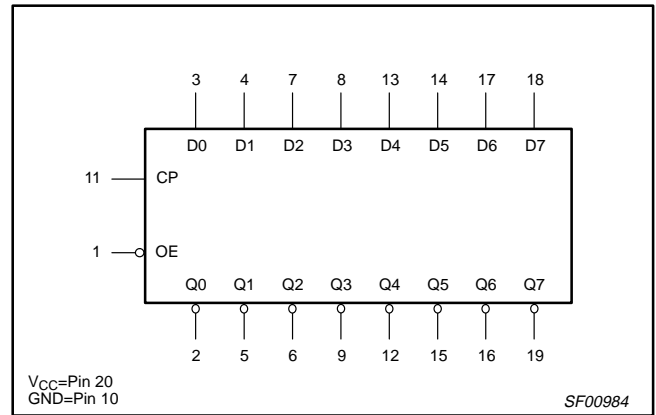
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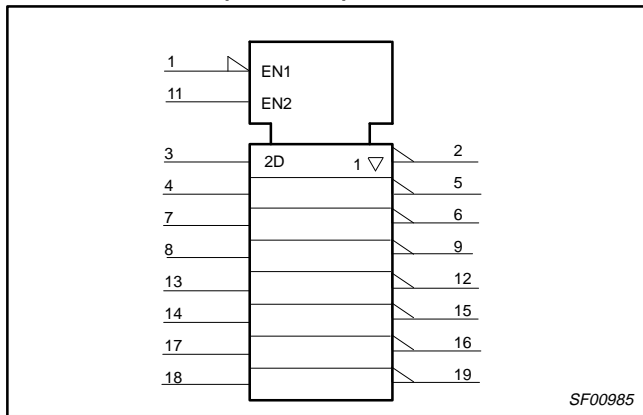
**LOGIC SYMBOL – 74F533**



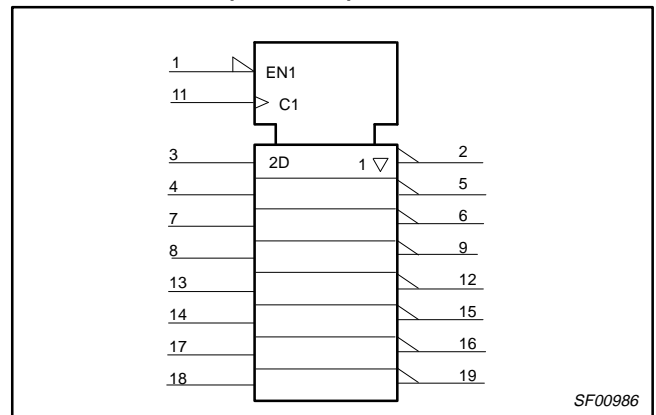
**LOGIC SYMBOL – 74F534**



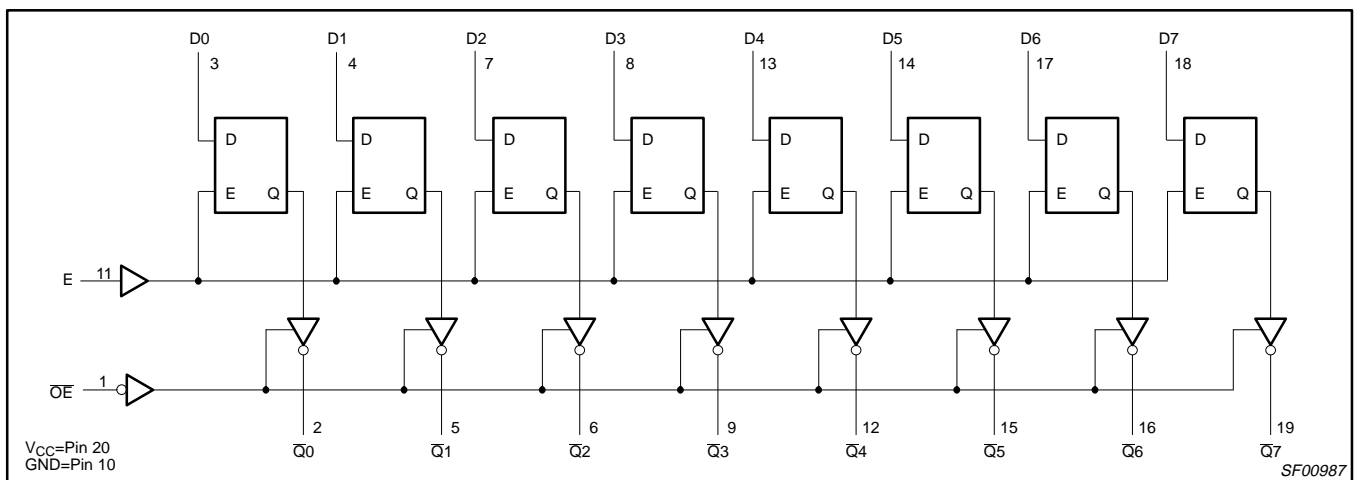
**LOGIC SYMBOL (IEEE/IEC) – 74F533**



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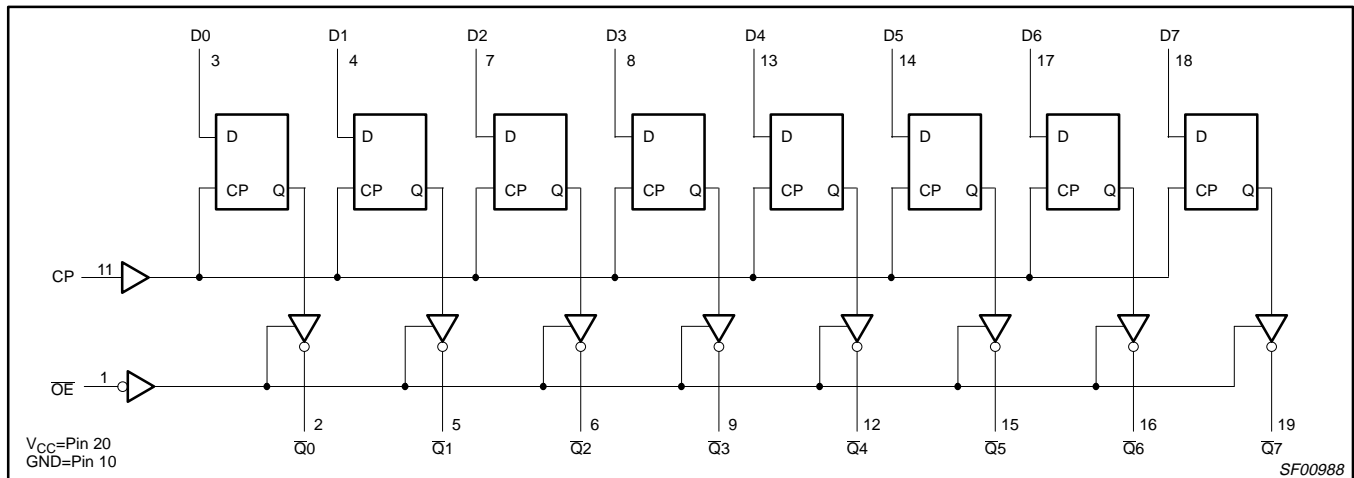
**LOGIC DIAGRAM – 74F533**



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## LOGIC DIAGRAM – 74F534



## FUNCTION TABLE – 74F533

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODES
OE	E	Dn		Q0 – Q7	
L	H	L	L	H	Load and read register
L	H	H	H	L	
L	↓	l	L	H	Enable and read register
L	↓	h	H	L	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

H = High voltage level  
 h = High voltage level one setup time prior to the High-to-Low E transition  
 L = Low voltage level  
 l = Low voltage level one setup time prior to the High-to-Low E transition  
 NC= No change  
 X = Don't care  
 Z = High impedance "off" state  
 ↓ = High-to-Low E transition

## FUNCTION TABLE – 74F534

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODES
OE	CP	Dn		Q0 – Q7	
L	↑	l	L	H	Load and read register
L	↑	h	H	L	
L	↯	X	NC	NC	Hold
H	↯	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

H = High voltage level  
 h = High voltage level one setup time prior to the Low-to-High clock transition  
 L = Low voltage level  
 l = Low voltage level one setup time prior to the Low-to-High clock transition  
 NC= No change  
 X = Don't care  
 Z = High impedance "off" state  
 ↑ = Low-to-High clock transition  
 ↯ = Not a Low-to-High clock transition

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5.0	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to + $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	48	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature	-65 to +125	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-3	mA
$I_{OL}$	Low-level output current			24	mA
$T_{amb}$	Operating free-air temperature range	0		70	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 10\%V_{CC}$	2.4		V	
			$\pm 5\%V_{CC}$	2.7	3.3	V	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.35	0.50	V
			$\pm 5\%V_{CC}$		0.35	0.50	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$			100	$\mu A$	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$			20	$\mu A$	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5V$			-0.6	mA	
$I_{OZH}$	Off-state output current, High-level voltage applied	$V_{CC} = \text{MAX}, V_O = 2.7V$			50	$\mu A$	
$I_{OZL}$	Off-state output current, Low-level voltage applied	$V_{CC} = \text{MAX}, V_O = 0.5V$			-50	$\mu A$	
$I_{OS}$	Short-circuit output current <sup>3</sup>	$V_{CC} = \text{MAX}$	-60		-150	mA	
$I_{CC}$	Supply current (total)	74F533	$V_{CC} = \text{MAX}$	$\overline{OE}=4.5V, D_n=E=GND$	41	61	mA
		74F534			$\overline{OE}=4.5V, D_n=GND$	51	86

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5V, T_{amb} = 25^\circ C$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			
			MIN	TYP	MAX	MIN	MAX		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dn to Q̄n	74F533	Waveform 2	4.0 3.0	6.0 4.5	8.5 7.0	4.0 3.0	9.5 8.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay E to Q̄n		Waveform 3	5.0 3.0	6.5 4.5	9.5 7.0	5.0 3.0	10.0 8.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 5.0	7.0 7.0	2.0 2.0	8.0 8.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time from High or Low level		Waveform 6 Waveform 7	2.0 2.0	3.5 3.0	6.0 5.5	2.0 2.0	7.0 6.5	ns
f <sub>MAX</sub>	Maximum Clock frequency	74F534	Waveform 1	150	165		135		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Q̄n		Waveform 1	3.0 3.0	4.5 4.5	7.0 7.0	2.5 2.5	7.5 7.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level		Waveform 6 Waveform 7	2.0 2.0	4.5 5.0	7.5 7.5	2.0 2.0	8.5 8.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time from High or Low level		Waveform 6 Waveform 7	2.0 2.0	3.5 3.5	6.5 5.5	2.0 2.0	7.5 6.5	ns

## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			
			MIN	TYP	MAX	MIN	MAX		
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, Dn to E	74F533	Waveform 4	1.5 0			1.5 0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, Dn to E		Waveform 4	2.5 2.5			2.5 2.5		ns
t <sub>w</sub> (H)	E Pulse width, High		Waveform 3	3.0			3.0		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, Dn to CP	74F534	Waveform 5	2.0 2.0			2.5 2.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, Dn to CP		Waveform 5	0 0			0 0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP pulse width, High or Low		Waveform 1	3.0 3.5			3.5 4.0		ns

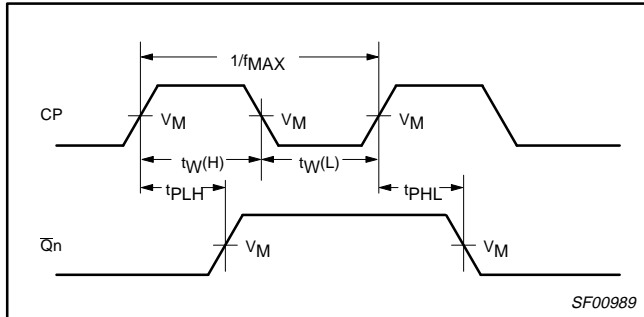
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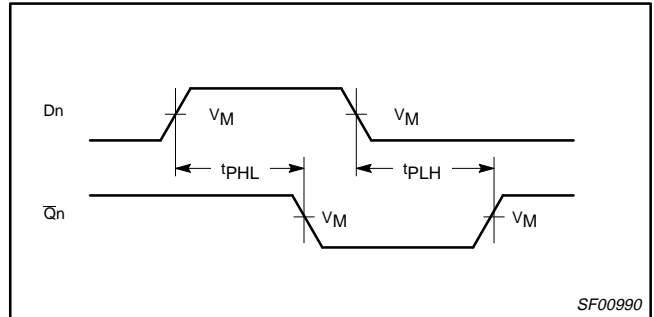
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$

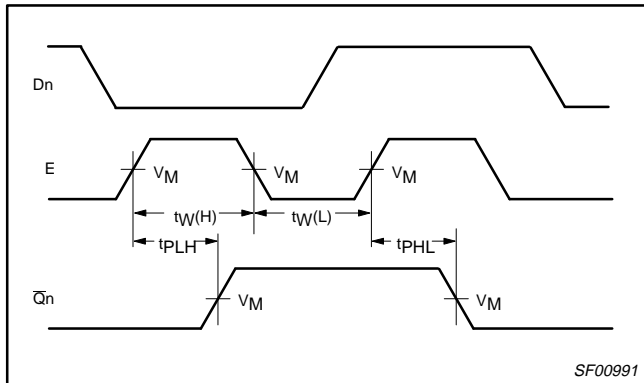
The shaded areas indicate when the input is permitted to change for predictable output performance.



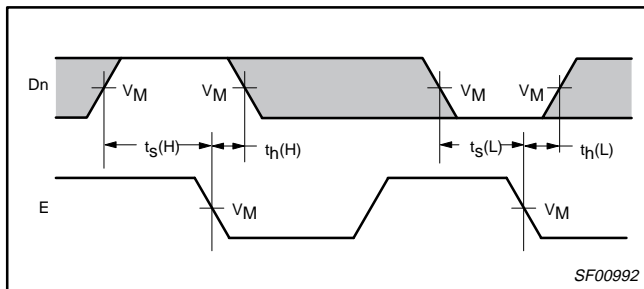
**Waveform 1. Propagation Delay, Clock and Enable Inputs to Output, Enable, Clock Pulse Widths, and Maximum Clock Frequency**



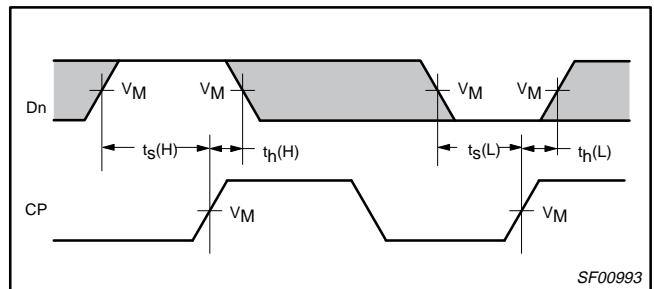
**Waveform 2. Propagation Delay for Data to Output**



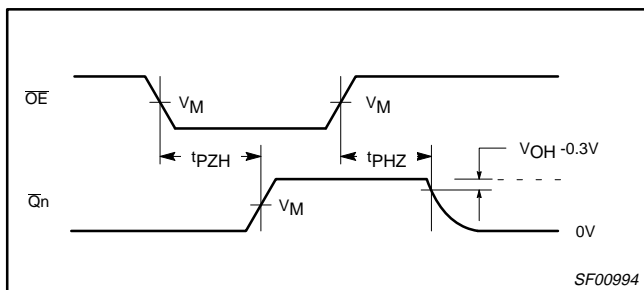
**Waveform 3. Propagation Delay, Enable Input to Output, and Enable Pulse Width**



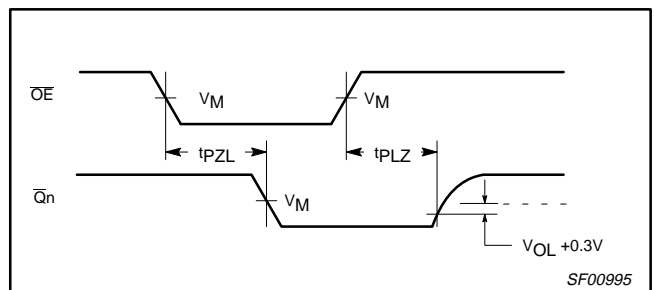
**Waveform 4. Data Setup and Hold Times**



**Waveform 5. Data Setup and Hold Times**



**Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level**

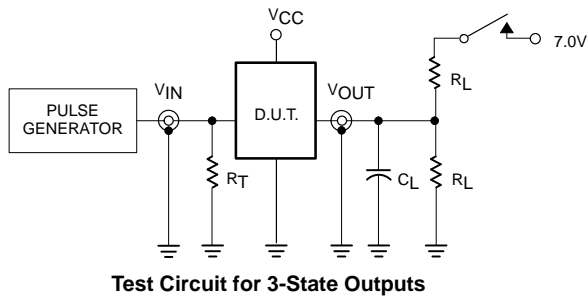


**Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

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## TEST CIRCUIT AND WAVEFORM



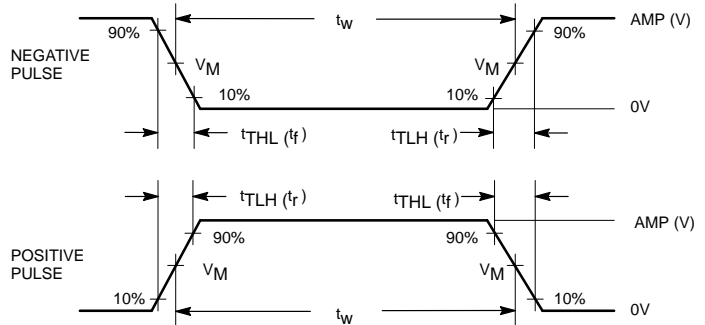
Test Circuit for 3-State Outputs

### SWITCH POSITION

TEST	SWITCH
$t_{pLZ}$	closed
$t_{pZL}$	closed
All other	open

### DEFINITIONS:

- $R_L$  = Load resistor; see AC electrical characteristics for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777