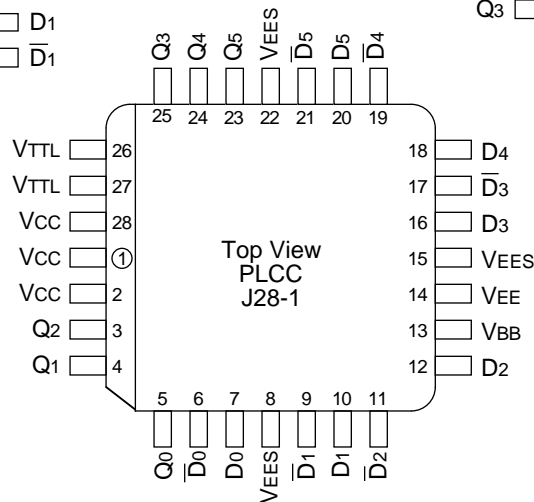
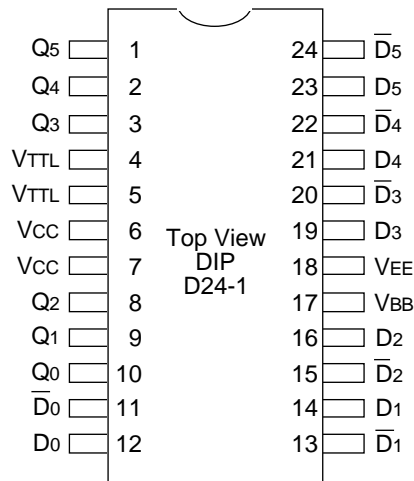


FEATURES

- Max. propagation delay of 3.7ns
- IEE min. of -37mA
- ESD protection of 2000V
- TTL outputs
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- 25% faster than National's 325
- Differential inputs with built-in offset
- Voltage and temperature compensation for improved noise immunity
- VBB output for single-ended use
- Internal 75KΩ input pull-down resistors
- Function and pinout compatible with National and Signetics (F100K)
- Available in CERDIP, CERPACK and PLCC

PIN CONFIGURATIONS



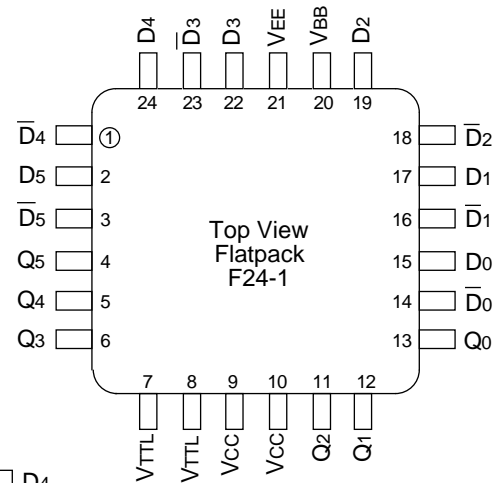
DESCRIPTION

The SY100S325 are hex translators for converting 100K ECL logic levels to TTL logic levels. Inputs can be used as inverting, non-inverting or differential receivers. An internal reference voltage generator provides VBB for single-ended operation or for use in Schmitt trigger applications. All inputs have 75KΩ pull-down resistors. The outputs will go LOW when the inputs are either open or have the same potential.

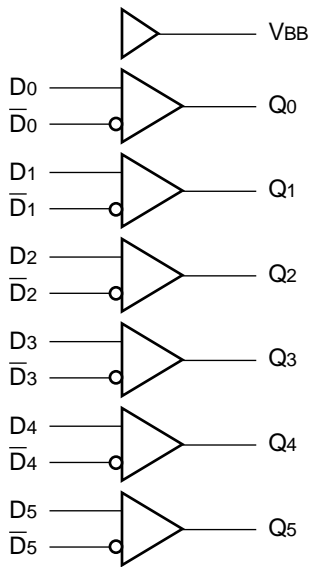
When used in single-ended operation, the apparent input threshold of the true inputs is 20mV to 40mV higher (positive) than the threshold of the complementary inputs. The VTTL and VEE power may be applied in either order.

PIN NAMES

Pin	Function
D0-D5	Data Inputs
D0-D5	Inverting Data Inputs
Q0-Q5	Data Outputs
VEES	VEE Substrate
VTTL	TTL Vcc Power Supply
VCCA	Vcco for ECL Outputs



BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -4.8V unless otherwise specified, VCC = VCCA = GND, VTTL = +4.5V to +5.5V, TA = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V _{OH}	Output HIGH Voltage	2.5	—	—	V	I _{OH} = -2.0mA	V _{IN} = V _{IH} (Max.)
V _{OL}	Output LOW Voltage	—	—	0.5	V	I _{OL} = 24mA	V _{IN} = V _{IL} (Min.)
V _{DIFF}	Input Voltage Differential	150	—	—	mV	Required for Full Output Swing	
V _{CM}	Common Mode Voltage	—	—	1.0	V	Permissible ±V _{CM} with Respect to V _{BB}	
I _{IH}	Input HIGH Current	—	—	350	μA	V _{IN} = V _{IH} (Max.), D ₀ -D ₅ = V _{BB} , D̄ ₀ -D̄ ₅ = V _{IL} (Min.)	
I _{IL}	Input LOW Current	0.5	—	—	μA	V _{IN} = V _{IH} (Min.), D ₀ -D ₅ = V _{BB}	
I _{OS}	Output Short Circuit Current	-150	-80	-60	mA	V _{OUT} = GND	
I _{EE}	VEE Power Supply Current	-37	-24	-17	mA	D ₀ -D ₅ = V _{BB}	
I _{TTL}	VTTL Power Supply Current	—	42	65	mA	D ₀ -D ₅ = V _{BB}	
V _{BB}	Ouptut Reference Voltage	-1380	-1320	-1260	mV	I _{VBB} = -2.1mA	
V _{IH}	Single-Ended Input HIGH Voltage	-1165	—	-880	mV	Guaranteed HIGH Signal for All Inputs (with One Tied to V _{BB})	
V _{IL}	Single-Ended Input LOW Voltage	-1810	—	-1475	mV	Guaranteed LOW Signal for All Inputs (with One Tied to V _{BB})	

AC ELECTRICAL CHARACTERISTICS

CERDIP

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tPLH tPHL	Propagation Delay Data to Output	1.0	2.2	3.0	ns	CL = 15pF, Figure 2
tPLH tPHL	Propagation Delay Data to Output	1.0	3.2	3.8	ns	CL = 50pF, Figure 2

PLCC/FLATPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tPLH tPHL	Propagation Delay Data to Output	900	2100	2900	ps	CL = 15pF, Figure 2
tPLH tPHL	Propagation Delay Data to Output	900	3100	3700	ps	CL = 50pF, Figure 2

SWITCHING WAVEFORM

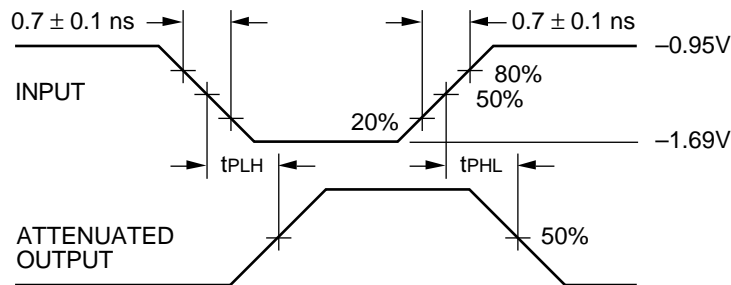


Figure 1. Propagation Delay

TEST CIRCUITS

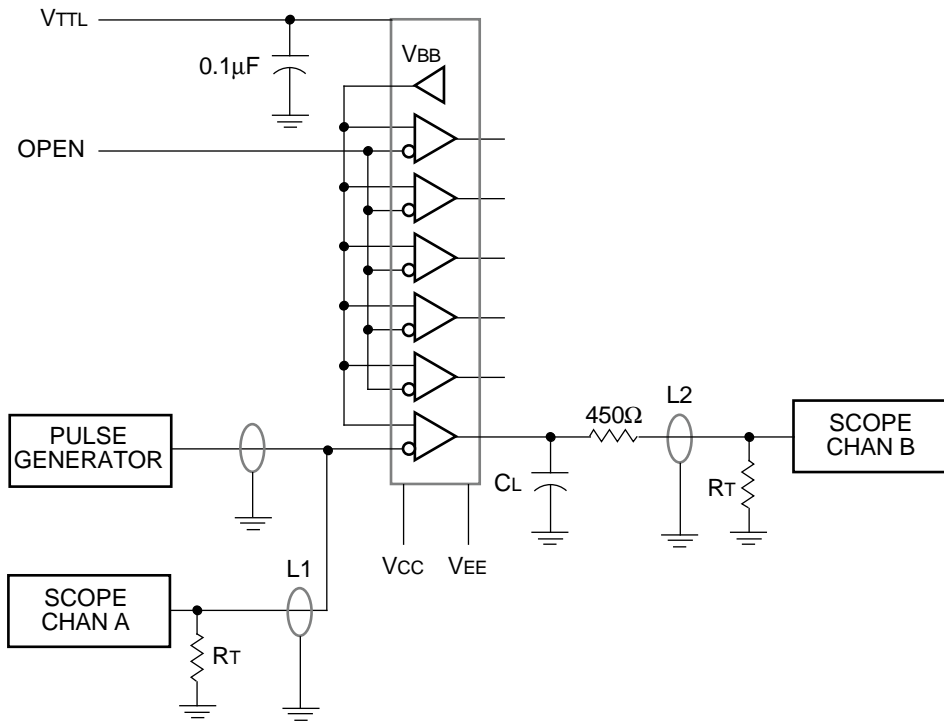


Figure 2. AC Test Circuit for 15pF Loading

NOTES:

VCC = 0V, VEE = -4.5V, VTTL = +5V

L1 and L2 = equal length 50Ω impedance lines

RT = 50Ω terminator internal to scope

Decoupling 0.1μF from GND to VCC, VEE and VTTL

All unused outputs are loaded with 500Ω to GND

CL = Fixture and stray capacitance = 3pF

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S325DC	D24-1	Commercial
SY100S325FC	F24-1	Commercial
SY100S325JC	J28-1	Commercial
SY100S325JCTR	J28-1	Commercial