External POR Circuit For CY7C960/961

This application note applies to CY7C960/961, all date codes.

Introduction
The CY7C960/961 has a problem with power supply glitches. If the supply voltage falls below rated Vdd, but does not go to 0 V, then unpredictable results may occur.

With the current design, the internal POR circuit does not discharge, and therefore does not reset and reassert itself when Vdd falls below legitimate operating range. This circuit is designed to eliminate POR problems associated with the CY7C960/ CY7C961. The circuit consists of two transistors and a voltage monitor attached to the 960/961 chip. If the monitor detects unusual power conditions, it is designed to discharge the Vdd pin to Vss, and then to reconnect Vdd to the supply rail. This allows the internal POR to operate correctly. The voltage monitor (MAXIM MAX708CPA/ MAX708CSA) compares the voltage on pin 2 (Vdd) to the threshold voltage on pin 6 (RESET IN), and sets its output RESET high if Vdd falls below RESET IN.

In normal operation, the 960/961 chip is powered by the supply through the P channel MOSFET to the Vdd pin. The RESET output of the MAX708 is used to bias the gates of the PMOS (Q1) and NMOS (Q2) transistors. When the supply voltage falls below a threshold, the RESET pin is driven high. This switches off the PMOS transistor (Q1) and switches on the NMOS transistor (Q2), thereby providing a low impedance path from the Vdd pin to Vss. This allows the internal POR circuit of the 960/961 to discharge. When the supply voltage rises above the threshold, RESET remains high for 200ms, and then goes low, switching off Q2 and switching on Q1, returning the 960/961 to normal operation.

Choosing Q1,Q2

Q1 Requirements
P-Channel, enhancement mode MOSFET
high current/ low rds(on)

\[ V_{gs(th)} : \]
\[ V_{gs} < V_{dd \text{ min} } - V_{OL} \]
\[ V_{dd \text{ min}} - V_{oh \text{ min}} < V_{gs}. \]
\[ V_{OL} = 0.4V, \text{ for } V_{cc} \text{ above trip } \]
\[ V_{dd \text{ min}} = 4.4V(ie \text{ trip point}) \]
\[ V_{oh \text{ min}} = 2.9V \]
\[ 1.5V < V_{gs(th)} < 4.0V. \]
\[ V_{gs(th)} = 3.0V \text{ is a safe value.} \]

\[ r_{ds(on)} : \]
\[ 5.0+/-.0.5V=\text{Supply Voltage-}I_{DS} \times r_{ds(on)}. \]

For supply = 5V nominal, and allowing I_{DS} to be 200mA for transients, then for 4.5V on the chip, \( r_{ds} < 2.5 \text{ Ohm} \)

Do not exceed this resistance value.

Q2 Requirements
N-Channel, enhancement mode MOSFET
high current/ low rds(on)

\[ V_{gs(th)} : \]
\[ \text{The minimum RESET output voltage of the MAX708 is rated at } V_{cc}-1.5V = 4.4-1.5 = 2.9V \text{ at trip point.} \]
\[ V_{gs(th)} < V_{oh \text{ min}} = 2.9V \]
\[ V_{gs(th)} = 2V \text{ is a safe value.} \]

\[ r_{ds(on)} : \]
Choose \( r_{ds(on)} \) for Q2 such that \( V_{ds(on)} < 100mV. \) For \( I = 100mA, r_{ds} < 1 \text{ Ohm} \)

\[ \text{NOTE. Choose } V_{gs(th)} \text{ of Q1, Q2 such that } V_{oh \text{ min}-V_{gs(th)}Q1} < V_{gs(th)Q2}, \text{ to avoid current spikes due to both transistors being on at the same time.} \]

\[ \text{NOTE. An Alternative MAXIM voltage monitor (MAX816) which has an adjustable threshold (by utilising a voltage divider) may be used.} \]
**Figure 1. External POR Circuit Diagram**

**Table 1: Bill of Materials**

<table>
<thead>
<tr>
<th>Item</th>
<th>P/N</th>
<th>Description</th>
<th>MFG</th>
<th>Cost</th>
<th>rds(on)</th>
<th>Vgs(th)</th>
<th>Idss(max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>MAX708CPA/CSA</td>
<td>Voltage monitor (8Pin DIL/SO)</td>
<td>Maxim</td>
<td>$5.13</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Q1</td>
<td>VP0300L</td>
<td>P Channel MOSFET Enhancement Mode</td>
<td>Vishay Siliconix</td>
<td>$0.97</td>
<td>2.2Ohm</td>
<td>3.1V</td>
<td>320mA*</td>
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<tr>
<td>Q2</td>
<td>BS170</td>
<td>N Channel MOSFET Enhancement Mode</td>
<td>National Semi</td>
<td>$0.33</td>
<td>1.2Ohm</td>
<td>2.1V</td>
<td>500mA</td>
</tr>
</tbody>
</table>

*Ids spike above Idss(max) is supplied by the bypass capacitor.*